Reg. No. | | | | | | | | | | | | |

Question Paper Code : 51444

B.E. /B. Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – Electronics and Communication Engineering Regulations 2009)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Simplify $f(x, y) = x'y + xy + xy'$.

2. Implement EXOR function using NAND gates only.

3. Design a Half Subtractor.

4. What is a parity bit ? Give the odd parity and even parity bits for the data 10.

5. State the difference between edge triggering and level triggering.

6. Give one application of a ring counter.

7. What is an EEPROM ?

8. State the difference between PAL and PLA.

9. What is a pulse mode asynchronous sequential circuit ?

10. What are the parts of a module in verilog ?

PART – B (5 × 16 = 80 Marks)

11. (a) (i) State and prove consensus theorem. **(6)**

(ii) Minimize the following function using Karnaugh Map : **(10)**

$f(A, B, C, D, E) = \Sigma m(0, 2, 5, 6, 8, 11, 12, 13, 16, 18, 20, 28, 30, 31)$

OR

(b) (i) State and prove De Morgan's theorem. **(6)**

(ii) Minimize the following function using Quine Mc Cluskey Method. **(10)**

$f(A, B, C, D, E) = \Sigma m(0, 1, 3, 5, 6, 7, 9, 10, 12, 13, 17, 19, 20, 25, 26, 29, 30)$

12. (a) (i) Design and explain the operation of a Carry Look-ahead adder. **(8)**

(ii) Design a 3 × 3 Binary (Array) Multiplier. **(8)**

OR

(b) (i) Explain the operation of a 8 ×1 Multiplexer and Implement the following function using a suitable Multiplexer **(8)**

$F(A, B, C, D) = \Sigma m(0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)$

(ii) Design a magnitude comparator to compare two 3-bit numbers : **8**

$A = A_2A_1A_0$ and $B = B_2B_1B_0$

13. (a) With logic diagram, characteristic table and characteristic equation explain the operation of a

(i) D Flip-Flop **(5)**

(ii) T Flip-Flop **(5)**

(iii) JK Flip-Flop **(6)**

OR

(b) (i) Design a 3-bit synchronous up/down Modulo 5 counter. **(8)**

(ii) With neat sketch, explain the operation of a 3-bit universal shift register. **(8)**

14. (a) (i) With timing waveforms, explain the memory read/write operation. (8)

(ii) What is memory expansion ? Explain. (8)

OR

(b) (i) Design a 3 × 8 decoder and Implement it using a suitable PLA. (8)

(ii) Design a 3-bit majority logic circuit and Implement it using a suitable PAL. (8)

15. (a) Design a sequence detector to detect the sequence 1010. Use the Algorithmic State Machine (ASM) Chart for the design. (16)

OR

(b) (i) What is an incompletely specified state machine ? Explain. (8)

(ii) Write the verilog code to realize a Full Adder using structural Modelling (Module instantiation). (8)

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Question Paper Code : 57288

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Fourth Semester

Electronics and Communication Engineering

EC 6405 – CONTROL SYSTEM ENGINEERING

(Common to Mechatronics Engineering and Medical Electronics Engineering)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Distinguish between open loop and closed loop control systems.
2. Write Mason's gain formula.
3. List the standard test signals used in time domain analysis.
4. State the effect of PI compensation in system performance.
5. What are the frequency domain specifications ?
6. What are M & N circles ?
7. State the necessary conditions for stability.
8. How will you find root locus on real axis ?
9. Define the state and state variable of a model system.
10. What is zero order hold circuit ?

PART – B (5 × 16 = 80 Marks)

11. (a) (i) What are the basic elements of mechanical rotational systems ? Write its force balance equations. **(4)**

(ii) Write the differential equations governing the mechanical translational system shown in figure 11(a)(ii) and determine the transfer function. **(12)**

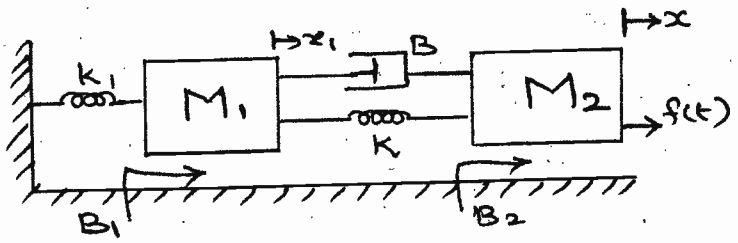

Figure 11(a)(ii)

OR

(b) Convert the block diagram shown in figure 11(b) to signal flow graph and find the transfer function using mason's gain formula. Verify with block diagram approach. **(16)**

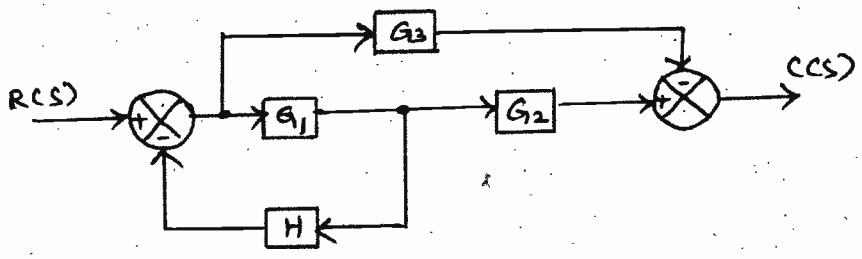

Figure 11(b)

12. (a) (i) Derive the time response of a first order system for unit step input. **(8)**

(ii) The unity feedback control system is characterized by an open loop transfer function G(s) = K / [s(s+10)]. Determine the gain K, so that the system will have damping ratio of 0.5 for this value of K. Determine the peak overshoot and peak time for a unit step input. **(8)**

OR

(b) With a neat block diagram and derivation explain how PI, PD and PID compensation will improve the time response of a system. **(16)**

13. (a) Sketch the Bode plot for the following transfer function and determine the system gain K for the gain cross over frequency to be 5 rad/sec.

$G(s) = Ks^2/[(1 + 0.2s)(1 + 0.02s)]$ **(16)**

OR

(b) (i) Write short notes on series compensation. **(4)**

(ii) Write down the procedure for designing Lead compensator using Bode plot. **(12)**

14. (a) (i) Using Routh Hurwitz criterion, determine the stability of a system representing the characteristic equation $S^6 + 2S^5 + 8S^4 + 12S^3 + 20S^2 + 16S + 16 = 0$ and comment on location of the roots of the characteristics equation. **(8)**

(ii) Describe about Nyquist Contour and its various segments **(8)**

OR

(b) A unity feedback control system has an open loop transfer function $G(s) = K/[s(s^2 + 4s + 13)]$. Sketch the root locus. **(16)**

15. (a) (i) Construct a state model for a system characterized by the differential equation $(d^3y/dt^3) + 6(d^2y/dt^2) + 11(dy/dt) + 6y + u = 0$ **(8)**

(ii) With the neat block diagram explain the sampled data control system and state its advantages. **(8)**

OR

(b) Test the controllability & observability of the system by any one method whose state space representation is given as **(16)**

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ -2 & -3 & 0 \\ 0 & 2 & -3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 2 \\ 0 \end{bmatrix} u \; ; \; y = [1\ 0\ 0] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$